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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,672	04/25/2000	Michael K. Brand	113337	9338

23838 7590 12/23/2005

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/557,672	BRAND ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment in RCE application filed on 09/28/2005. Claims 1-23 are pending in the action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Tegethoff, Mauro, US patent no. 5,539,652.

As per claim 1, Tegethoff anticipates a method for manufacturing test simulation in electronic circuit design with feature limitations very identical to the claimed invention (Abstract and Field of the Invention). According to Tegethoff, the method includes steps:

Performing testing data for a product to a point of product failure to collect stress testing data, the stress testing data representing the response of the product operating in a first environment (col. 6, line 59 to col. 7, line 9, col. 10, lines 16-33, col. 27, line 55 to col. 29, line 5, col. 40),

Calculating the mean time between failures or lifetime for the product operating in a second environment with different operating conditions based on the accelerated

stress testing data in determining product reliability as claimed (cols. 6-10, cols. 27-29, 39-40).

As per claim 2, Tegethoff anticipates various working environments being used to analyze or predict failure time (cols. 6-10).

As per claim 3, Tegethoff anticipates stress data derived from stress environment, temperature tests, stress conditions, etc before the test product fails.

As per claims 4-7, Tegethoff anticipates various stress tests or different test loads to test product life cycle (cols. 6-10, 39-40, 46, for example).

As per claim 8, Tegethoff anticipates test specification for user application such as for the claimed BOM test.

As per claims 9-11, Tegethoff anticipates the stress test during product design cycle, manufacturing, applications for commercial use, computer test, etc.

As per claims 12-14, Tegethoff anticipates a method for manufacturing test simulation in electronic circuit design with feature limitations very identical to the claimed invention (Abstract and Field of the Invention). According to Tegethoff, the method includes steps:

Performing testing data for a product to a point of product failure to collect stress testing data, the stress testing data representing the response of the product operating in a first environment (col. 6, line 59 to col. 7, line 9, col. 10, lines 16-33, col. 27, line 55 to col. 29, line 5, col. 40),

Calculating the mean time between failures for the product operating in a second environment based on the accelerated stress testing data as claimed. Biggs discloses

stress history data and a variety of test loads or all the stresses in determining product reliability (cols. 6-10, cols. 27-29, 39-40).

As per claim 15, Tegethoff anticipates mean time between failures for various loading conditions or working environment as claimed (cols. 40-46).

As per claims 16-21, Tegethoff discloses test data, stress testing, temperature tests, vibration tests, and a computer system for implementation computation algorithm to compute failure time of the product design for various working conditions as claimed.

As per claims 22-23,Tegethoff anticipates a method and system for manufacturing test simulation in electronic circuit design with feature limitations very identical to the claimed invention (Abstract and Field of the Invention). According to Tegethoff, the method includes steps:

Performing testing data for a product to a point of product failure to collect stress testing data, the stress testing data representing the response of the product operating in a first environment (col. 6, line 59 to col. 7, line 9, col. 10, lines 16-33, col. 27, line 55 to col. 29, line 5, col. 40),

Calculating the mean time between failures or product lifetime for the product operating in a second environment with product design change or redesign part or component as claimed to account for environment change, for example, based on the accelerated stress testing data as claimed reliability (cols. 6-10, cols. 27-29, 39-40).

As per claim 23, Tegethoff anticipates a stress test environment with accelerated conditions such as a temperature stress, a thermal test, operating condition test, etc.

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,491,528, issued to McLean, Harry, on Dec. 2002
2. US patent no. 6,541,394, issued to Chen et al, on Apr. 2003
3. US patent no. 6,546,507, issued to Coyle et al, on Apr. 2003

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dec. 15, 2005

Thai Phan
Patent Examiner
Art Unit: 2128